ABSTRACT

A bus bridge is defined to provide an interface between two AHB buses. These busses normally have separate requirements but both must provide high performance. The first is for transfer of data from CPU to memory and peripherals. The second is to support the transfer of a large amount of data by a single peripheral to local memory or other local peripherals. The AHB-to-HTB bus bridge provides a means for the interfacing these two separate AHB buses allowing communication between them and securing data integrity. The bus bridge of this invention is defined to be an AHB memory bus slave but a high performance data transfer bus master.